IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Hugo Cheung
Serial No.: 10/650,403
Filed: 08/28/03

Art Unit: 2182
Examiner: Tanh Q. Nguyen
Docket: TI-32740.1
Conf. No.: 6534

For: SERIAL PERIPHERAL INTERFACE WITH HIGH PERFORMANCE BUFFERING SCHEME

RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF

Claim 18 is not included in the Claims Appendix because claim 18 is not involved in the appeal.

APPELLANTS' AMENDED BRIEF UNDER 37 C.F.R. §1.192

Board of Patent Appeals and Interferences
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The following amended Appeal Brief is respectfully submitted in connection with the above-identified application in response to the Notification of Non-Compliant Appeal Brief mailed October 31, 2007. Please charge all required fees, including any extension of time fees, to the deposit account of Texas Instruments Incorporated, Deposit Account No. 20-0668.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, to whom this application is assigned.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Applicant's legal representative.

STATUS OF THE CLAIMS

Claims 15-17, 19, and 20 are the subject of this appeal. Claims 15-20 are rejected. Claims 1-14 and 21 have been canceled. This application was filed on August 28, 2003.

STATUS OF THE AMENDMENTS

The Appellants filed an amendment under 37 C.F.R. § 1.116 on September 25, 2006 in response to the Office Action dated June 23, 2006. The amendment was not entered.

SUMMARY OF CLAIMED SUBJECT MATTER

Specification page 15, line 12 to page 16, line 16, provides a concise explanation of the invention defined in independent claim 15.

In accordance with this example, prior to operation, the FIFO buffer 400 is empty and without remaining data to be transmitted or received, and all counters and pointers are configured to the same location, for example, all pointers and counters could be pointing to zero (0000B or 0 decimal). During an initialization step 502, the CPU will write to an SPI data register, for example, SPI data register 314, and the SPI configuration will facilitate the writing of data into the location of FIFO buffer 400 designated by the WrPtr pointer. Thereafter, in a transmit buffering step 504, the WrPtr pointer is suitably incremented to prevent the next byte to be transmitted from overwriting the previous written byte, while the WrShfCnt counter is incremented to keep track of the number of bytes available for transmission For example, in the illustration of Figure 4, with WrPtr equal to 8 decimal, and ShfPtr equal to 3 decimal, WrShfCnt is equal to 5 decimal, indicating 5 bytes are available for writing.

Upon the writing of data to an SPI data register in step 502, and incrementing of the WrPtr pointer and the WrShfCnt counter in step 504, a transmit and receive shifting step 506 can be provided. In step 506, the SPI configuration 300 can begin transmitting the data by reading the data from the ShfPtr location in the buffer, and then writing the data to the transmit shift register 302. Upon completion of transferring of data from FIFO buffer 308 to the transmit shift register 302, shifting of the registers can suitably occur.

At the same time that transmission of data is being completed, or substantially immediately after transmission of data, for example, within one clock cycle, a new byte of data can be suitably received and stored in the receive shift register 304, i.e., stored in the location of FIFO buffer 400 designated by the RdPtr pointer. Accordingly, by providing a buffering scheme that permits data to be received substantially at the same time, or immediately after, the transmitting of data, a high data rate can be obtained, for example, up to 12 Mhz or more.

After the transmission and receiving of data in steps 504 and 506, a receive buffering step 508 can be suitably provided. In step 508, the ShfPtr pointer can again be incremented, and thus point to a new location in the FIFO buffer 400. In addition, the RdShfCnt can also be suitably incremented to indicate that the SPI configuration 300 has received another byte of data.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Rejection under 35 USC § 103(a) as being unpatentable over U.S. Patent No. 5,278,956 in view of U.S. Patent Application Pub. No. US 2002/0078317 A1.

ARGUMENT

Rejection under 35 USC § 103(a) over U.S. Patent No. 5,278,956 in view of U.S. Patent Application Pub. No. US 2002/0078317 A1.

Claims 15-17, 19, and 20

Claim 15 includes "... initializing a single buffer to act as transmitter and receiver by writing data to a data register; ... performing a transmit and receive shifting sequence to facilitate transmitting of the data and receiving of new data at substantially the same time ...". The references of record do not show, teach, or suggest the above recited limitations of claim 15. U.S. Patent Application Pub. No. US 2002/0078317 A1 does not disclose a single buffer to facilitate transmitting and receiving at substantially the same time. The references do not teach how the device of U.S. Patent Application Pub. No. US 2002/0078317 A1 can be combined with U.S. Patent No. 5,278,956 to obtain a single buffer for performing a transmit and receive shifting sequence to facilitate transmitting of the data and receiving of new data.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 15-17, 19, and 20 is improper, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejection.

Please charge any fees necessary in connection with the filing of this paper, including any necessary extension of time fees, to Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,

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CLAIMS APPENDIX

15. A high performance buffering technique for use with a serial peripheral interface to facilitate high data rates, said buffering technique comprising the steps of

initializing a single buffer to act as transmitter and receiver by writing data to a data register;

performing a transmit buffering sequence to prepare for the transmitting of the data;

performing a transmit and receive shifting sequence to facilitate transmitting of the data and receiving of new data at substantially the same time; and

performing a receive buffering sequence to prepare for the receipt of additional new data.

16. The high performance buffering technique of claim 15, wherein said initialization step comprises the step of:

writing the data into a location of said buffer as designated by a write pointer.

17. The high performance buffering technique of claim 15, wherein said transmit buffering sequence comprises the steps of:

incrementing a write pointer to prevent a next byte to be transmitted from overwriting a previous written byte; and

incrementing a write shift counter to facilitate tracking of a number of bytes available for transmission.

18. The high performance buffering technique of claim 15, wherein said transmit and receive shifting sequence comprises the steps of:

reading the data from a location in the buffer designated by a shift pointer;

writing the data to a transmit shift register;

shifting of the transmit shift register; and

receiving and storing the new data in a receive shift register in a location of said buffer designated by a read pointer.

19. The high performance buffering technique of claim 15, wherein said receive buffering sequence comprises the steps of:

incrementing a shift pointer to identify a new location in the buffer for receiving data; and

incrementing a read shift counter to indicate that the new data has been received.

20. The high performance buffering technique of claim 15, wherein said buffering technique further comprises the steps of:

interrupting a CPU if the data is ready for transmitting and said buffer is approximately full; and

interrupting the CPU if said buffer is ready to receive data and said buffer is approximately empty.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.